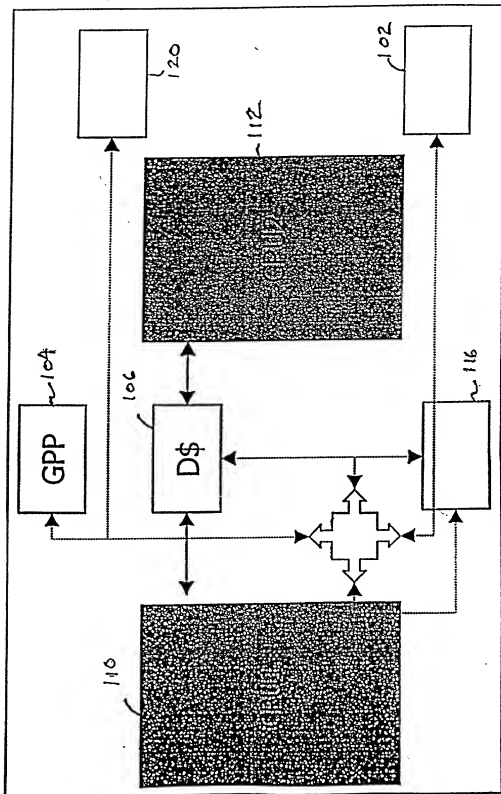


UPA-N, 1.6 GB/s

100



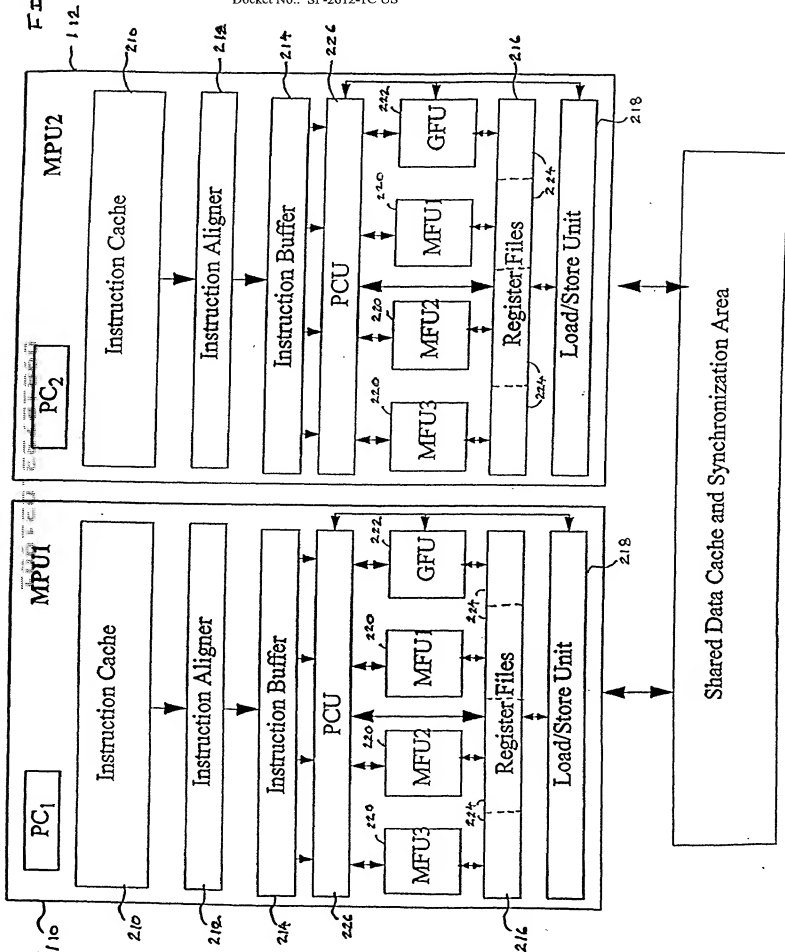
Title: EFFICIENT HANDLING OF A LARGE REGISTER  
FILE FOR CONTEXT SWITCHING  
Inventors: Marc Tremblay; William Joy  
Docket No.: SP-2612-1C US

1c979 U.S. PTO  
09/812733



03/19/01

FIG. 2



Broadcast Writes (5)

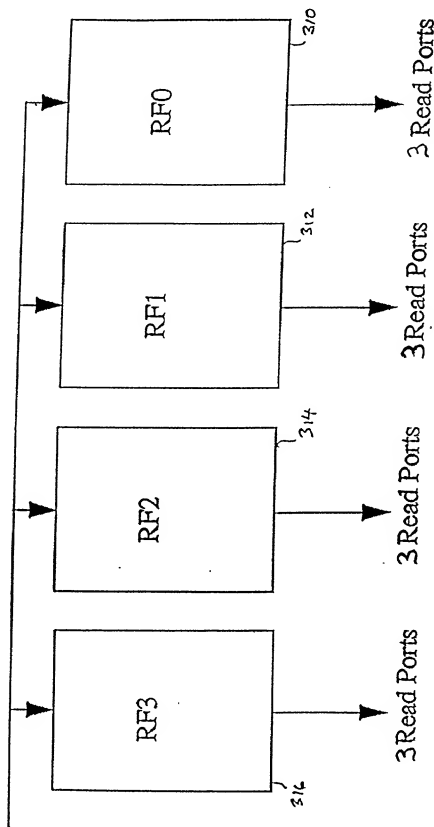


FIGURE 3 .Logical register file physically split in four coherent parts.

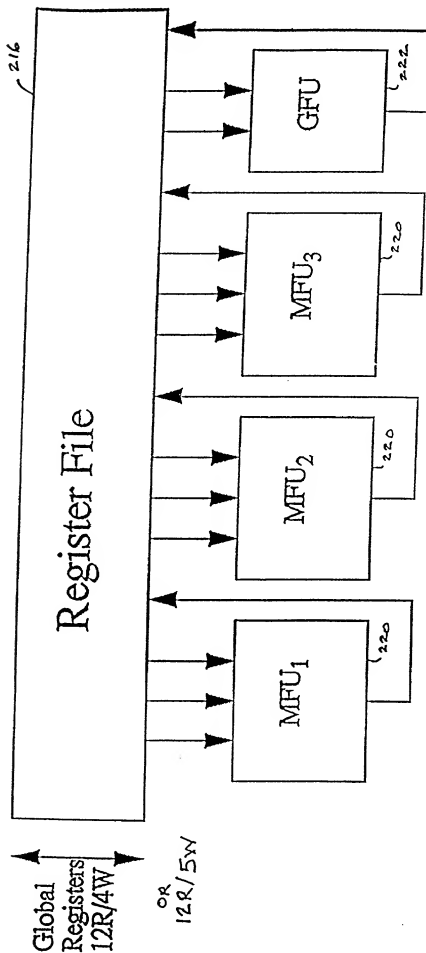


FIGURE 4. Logical view of the register file to the compiler/programmer.

Title: EFFICIENT HANDLING OF A LARGE REGISTER  
FILE FOR CONTEXT SWITCHING

Inventors: Marc Tremblay; William Joy

Docket No.: SP-2612-1C US

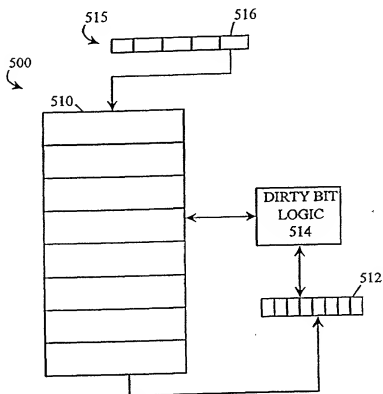


FIG. 5

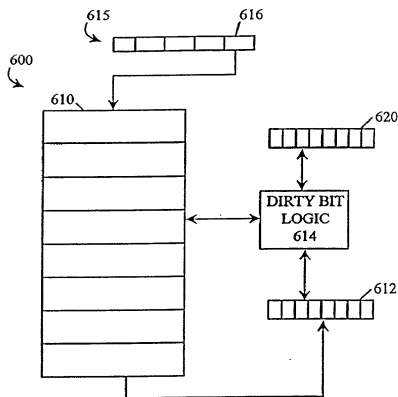
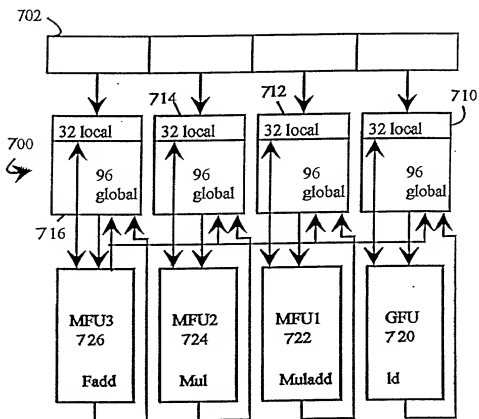


FIG. 6

FIG. 7



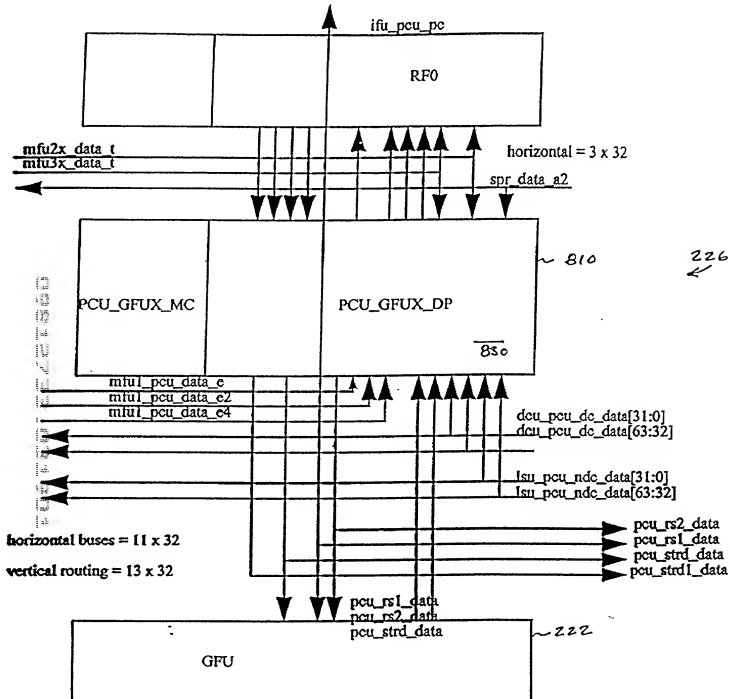


FIGURE 8A Channel congestion above and below pcu\_gfux\_dp block



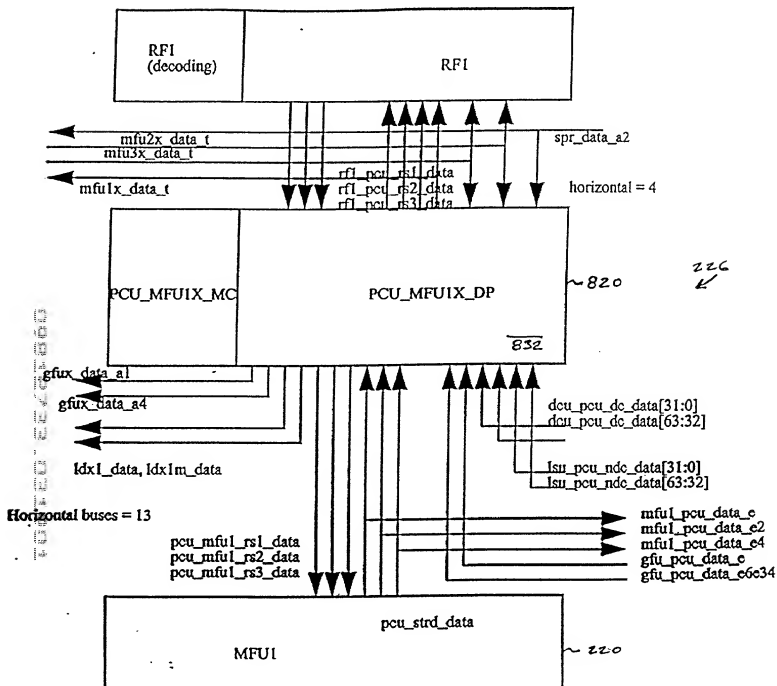


FIGURE 8B Channel congestion above and below pcu\_mful\_x\_dp block

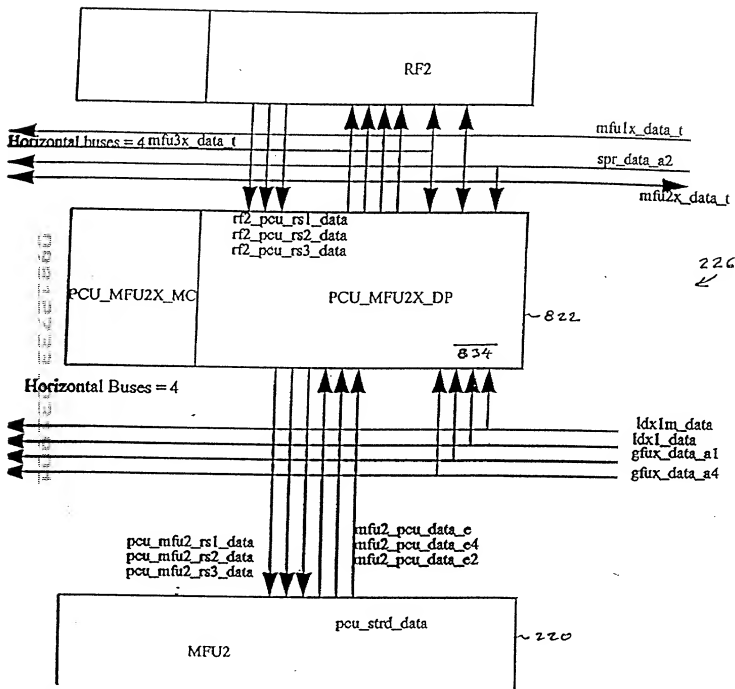
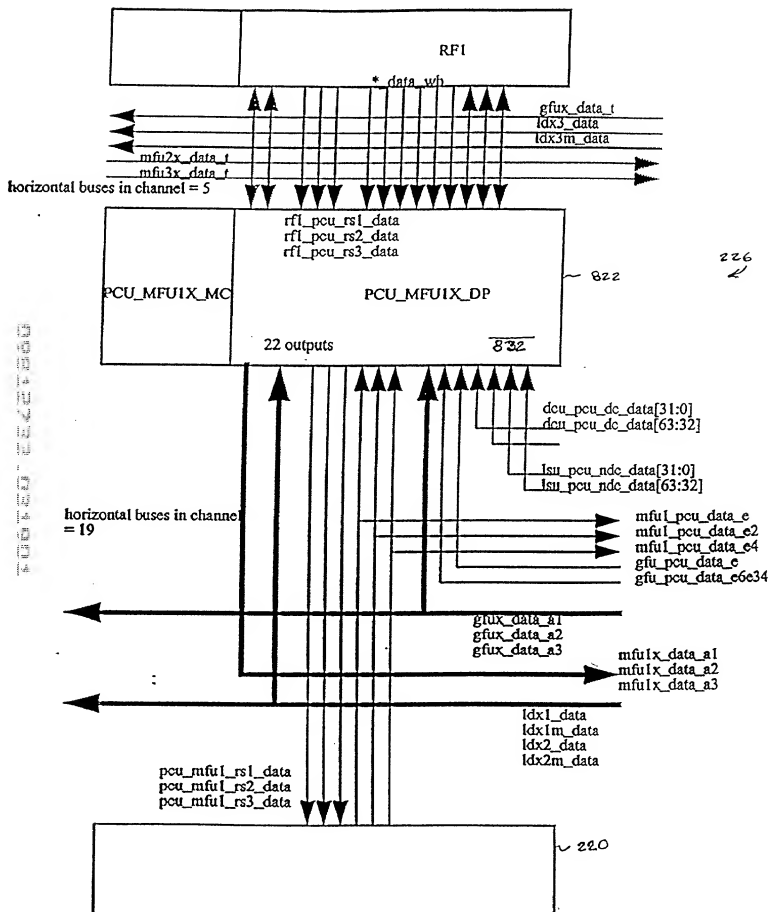


FIGURE 8C Channel congestion above and below pcu\_mfu2x-dp block

FIG. 8D



Internal Registers of PCU

Register name	width	address specifier	user access	supervisor access	thread state
PSR	8	010_0001	no	rd/wr	yes
TPSR1	8	010_0010	no	"	yes
TPSR2	8	010_0011	no	"	yes
PCR	7	010_0000	no	"	no
TL	2	010_0100	no	"	no
TICK	32	010_0101	read only	"	no
TVALUE	32	010_0110	no	"	no
TCNTL	8	010_0111	no	"	no
GX	13	001_0000	no	rd only	yes
INT	7	010_1000	no	rd/wr	yes
FSR	16	001_0001	rd/wr	"	yes
FMT	2	010_1010	rd/wr	rd/wr	yes
DIRTY	6	010_1011	rd/wr	"	yes
INT_OTHER	.	010_1001	no	wr only	yes

FIG. 9

Processor Control Register (PCR)

PCR [0]	PCR POW	Description power management	Initial value 0 (off)	After a trap N/C not changed
[1]	ICE	icache enable	0	"
[2]	DCE	dcache enable	0	"
[3]	BPTC	branch predict taken enable	0	"
[4]	PE	pipeline enable	0	"
[5]	MSTEP	memory step	0	"
[6]	PID	processor ID	hard- wired	hardwired

FIG. 10

Instruction	Instruction
vliw_1	setir ra, PSR
vliw_2	ld_2 [r1+r2], r3
vliw_3	ld_3
vliw_4	ld_4
vliw_5	ld_5
vliw_6	ld_6

FIG. 11A

cycle	1	2	3	4	5	6	7	8	9	10	11	12
setir	D	E	A1	A2	A3	T	WB					
ld_2		D	E	A1	A2	A3	T	WB				
ld_5						D	E	E				
ld_7												

1122

1144

1150

1124

FIG. 11B

Instruction	Instruction
vliw_1	setir ra, PCR
vliw_2	inst2
vliw_3	inst3
vliw_4	inst4
vliw_5	inst5
vliw_6	inst6
vliw_7	inst7
vliw_8	inst8
vliw_9	setir rb, PSR
vliw_10	inst10
vliw_11	inst11

FIG. 12A

	1	2	3	4	5	6	7	8	9	10	11	12	13
cycle	T	WB											
setir													
inst7		D	D	E	A1	A2	A3	T	WB				
inst8				D	D	D	D	D	D	D	E	A1	A2
setir											D	D	D
IST		ST		ST	ST	ST	ST	ST	ST		ST	ST	ST

FIG. 12B

	14	15	16	17	18	19	20	21	22	23	24	25	26
cycle	A3	T	WB										
inst8													
setir	D	D	D	D	E	A1	A2	A3	T	WB			
inst10					D	D	D	D	D	D	E	A1	A2
inst11											D	E	A1
ST	ST	ST	ST		ST	ST	ST	ST	ST				

Dirty Register

	Unit	rd [6:5]
[0]	all	01
[1]	all	10
[2]	gfu	11
[3]	mfu1	11
[4]	mfu2	11
[5]	mfu3	11

FIG. 13



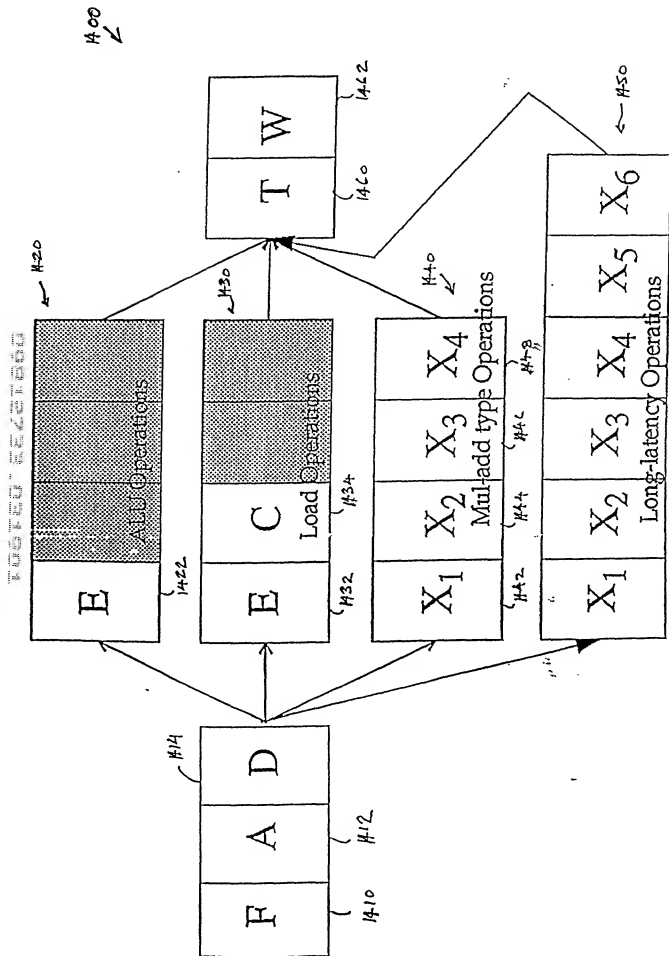


FIGURE 4. Pipeline diagram.